M 2038

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2006.

Third Semester

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Common to BE (PT) Second Semester R 2005 Electronics and Communication Engineering)

(Regulation 2004)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert 1110011 into hexadecimal through octal.

2. What is the feature of Gray code?

3. Write down fan in and fan out of a standard TTL IC.

4. Represent a half adder in block diagram form and also its logic implementation.

5. What is the drawback of SR flip flop? How is this minimized?

6. What is a sequence generator?

7. What is an asynchronous sequential circuit?

8. Draw a scale of 8 ripple counter.

9. What is meant by 'static' and 'dynamic' memories?

10. How is individual location in a EEPROM programmed or erased?

PART B — (5 × 16 = 80 marks)

11. (i) Prove by perfect induction :

(1) $A + AB = A$

(2) $A(A + B) = A$

(3) $A + A'B = A + B$ and

(4) $A(A'+B) = AB$. (8)

(ii) Reduce the following function using K map : $f = ABC' + A'B'C + ABC + AB'C$ and realize using NAND gates only. (8)

12. (a) Draw the symbol, truth table and the equation of the three basic gates and two universal gates and realize all the five gates using either of the universal gates. (16)

Or

(b) (i) Draw a CMOS NAND gate and explain its operation. What are the characteristics of CMOS? (10)

(ii) Draw a tristate TTL gate and explain its operation. (6)

13. (a) (i) Draw an asynchronous decade counter and explain its operation drawing neat waveforms. (8)

(ii) Draw a 3 bit reversible counter and explain its operation. (8)

Or

(b) (i) Draw a 4 bit serial in serial out shift register and draw its waveforms. (8)

(ii) Draw a 4 bit parallel in serial out shift register and briefly explain. (8)

14. (a) Design a circuit with inputs A and B to give an output Z = 1 when AB = 11 but only if A becomes 1 before B, by drawing total state diagram, primitive flow table and output map in which transient state is included. (16)

Or

(b) Design a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z = 1 it will remain so until A goes to 0. Draw waveform diagram, total state diagram, primitive flow table for designing this circuit. (16)

15. (a) (i) How can one make 64 × 8 ROM using four 32 × 4 ROMs? Draw such a circuit and explain. (8)

(ii) Implement binary to excess 3 code converter using ROM. (8)

Or

(b) Draw a dynamic RAM cell and explain its operation. Compare its simplicity with that of NMOS static RAM cell, by way of diagram and operation. (16)